

Notice of References Cited

Application/Control No.

09/668,320

Applicant(s)/Patent Under
Reexamination
ALPERT ET AL.

Examiner

Morella I Rosales-Hanner

Art Unit

2128

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,347,393	02-2002	Alpert et al.	716/2
	B	US-			
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	F	US-			
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*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Curtis L. Ratzlaff, Satyamurthy Pullela and Lawrence T. Pillage, "Modeling the RC-Interconnect Effects in a Hierarchical Timing Analyzer", IEEE 1992 Custom Integrated Circuits Conference, Pgs 15.6.1 - 15.6.4.□□
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	W	Charles J. Alpert, Anirudh Devgan and Stephen T. Quay, "Buffer Insertion with Accurate Gate and Interconnect Delay Computation", DAC '99, Pgs 479 - 484□□
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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